tation process is intended to form the P-type channel region **7** that has a dopant concentration much lower than the moderate dopant concentration of the N-doped polysilicon gate structure **5**, and that the first section **51** will be further doped using N-type dopant to have a high N-type dopant concentration in the subsequent step 5' as described below, the P-type ions implanted in this step is considered to have no impact on the intended characteristics of the first section **51** of the polysilicon gate structure **5**.

[0052] Preferably, the P-type ions are implanted with a certain inclination (as indicated by arrows) to facilitate the lateral extension of the channel region **7** under the silicon oxide layer **4** and in contact with the drift region **3**.

[0053] In step 5', referring to FIG. **3***e*, a source/drain implantation process is employed to implant ions of an N-type dopant through the opening D, which is preferred to be arsenic, using the remainder of the photoresist layer **6** as a mask, thereby forming a source region **8** in the exposed portion of the epitaxial layer **2** and causing the exposed first section **51** of the polysilicon gate structure **5** to have a high N-type dopant concentration. As a result, the channel region **7** shrinks to a region sandwiched between the source region **8** and the drift region **3**, and the second section **52** of the polysilicon gate structure **5** covered by the remainder of the photoresist layer **6** remains moderately-doped.

[0054] Preferably, the N-type ions are perpendicularly implanted in the source/drain implantation process at a dose of 1×10^{15} atoms/cm^2 to 1×10^{16} atoms/cm^2 and the first section **51** of the polysilicon gate structure **5** has a high dopant concentration of 1×10^{20} atoms/cm^3 to 1×10^{21} atoms/cm^3.

[0055] Preferably, the first section **51** exposed in the opening D has a width equal to half of a width of the polysilicon gate structure **5**.

[0056] In both the first and second embodiments, the method may further include subsequent steps of: depositing a metal layer over the whole resulting substrate; and annealing the structure at a high temperature to form metal silicide along where the metal layer comes in contact with silicon and polysilicon, i.e., top surfaces of the source region **8**, the sinker region **12**, the polysilicon gate structure **5**, the gate shield layer **11** and the drain region **9**. Alternatively, the source and sinker regions **8**, **12** may also be connected to external circuits through a metal on the backside of the substrate.

[0057] In other embodiments, the method is employed to fabricate a P-channel RF LDMOS device by forming in the nine steps components similar to those of the above described embodiments except each having an opposite conductivity type. For example, in this embodiment, a heavily-doped N-type silicon substrate, optionally formed thereon with a lightly-doped N-type epitaxial layer is provided in step 1 or 1'; in step 2 or 2', ions of a P-type dopant are implanted, with boron being preferred; in step 3 or 4', ions of an N-type dopant are implanted, preferably phosphorus or arsenic; and in step 4 or 5', ions of a P-type dopant are implanted, which is preferred to be boron.

[0058] Similarly, as can be seen from FIG. **4***a*, an RF LDMOS device fabricated using the method of the present invention has a non-uniformly doped polysilicon gate structure **5** consisting of a heavily-doped first section **51** and a moderately-doped second section **52**. As described above, such structure leads to different depletion region widths w**1** and w**2** of the first and second sections **51** and **52**, as shown in FIG. **4***b*, which enables the RF LDMOS device to have an improved HCI effect without increasing the on-resistance.

[0059] It is to be understood that the preferred embodiments of the present invention presented in the foregoing description are not intended to limit the invention in any way. Those skilled in the art can make various alterations, modifications, and equivalent alternatives without departing from the scope of the invention. Thus, it is intended that the present invention covers all such alterations, modifications, and equivalent alternatives that fall within the true scope of the invention.

What is claimed is:

1. A radio frequency (RF) laterally diffused metal oxide semiconductor (LDMOS) device comprising: a gate structure on a surface of a substrate; and a source region and a drain region beneath the surface of the substrate, the source region and the drain region formed on opposite sides of the gate structure, wherein the gate structure comprises a first section proximal to the source region and a second section proximal to the drain region, and wherein the first section of the gate structure has a dopant concentration at least one decimal order higher than a dopant concentration of the second section of the gate structure.

2. The RF LDMOS device of claim **1**, wherein each of the first section and the second section has a width equal to half of a width of the gate structure.

3. The RF LDMOS device of claim **1**, wherein the first section of the gate structure is heavily doped with a dopant concentration of 1×10^{20} to 1×10^{21} atoms/cm^3 and the second section of the gate structure is moderately doped with a dopant concentration of 1×10^{18} to 1×10^{19} atoms/cm^3.

4. A method of forming a radio frequency (RF) laterally diffused metal oxide semiconductor (LDMOS) device comprising:

forming a gate structure on a surface of a substrate and forming a source region and a drain region beneath the surface of the substrate, wherein the source and drain regions are formed on opposite sides of the gate structure; and

doping the gate structure to make a first section of the gate structure proximal to the source region have a dopant concentration at least one decimal order higher than a dopant concentration of a second section of the gate structure proximal to the drain region.

5. The method of claim **4**, wherein each of the first section and second section has a width equal to half of a width of the gate structure.

6. The method of claim **5**, wherein doping the gate structure comprises:

performing a first doping process on both of the first section and the second section; and

covering the second section with a photoresist and performing a second doping process only on the first section to make the first section have a dopant concentration at least one decimal order higher than a dopant concentration of the second section.

7. The method of claim **6**, wherein the first doping process is performed prior to the second doping process and after forming the gate structure.

8. The method of claim **6**, wherein the first doping process is an in-situ doping process performed during forming the gate structure.

9. The method of claim **4**, wherein the first section of the gate structure is heavily doped with a dopant concentration of 1×10^{20} atoms/cm^3 to 1×10^{21} atoms/cm^3 and the second section of the gate structure is moderately doped with a dopant concentration of 1×10^{18} atoms/cm^3 to 1×10^{19} atoms/cm^3.

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